Staff Analogue IC Design Engineer - High-Speed Custom Logic

Job Specification

About Optalysys

Optalysys is a pioneering UK and US based deep-tech company developing new ways to power the future of computing. By harnessing light, we are creating advanced photonic technologies that help the world's most demanding systems run faster and more efficiently. Our work supports breakthroughs in areas such as artificial intelligence, cybersecurity and scientific discovery. At Optalysys, we're bringing together talented people who are passionate about building technology that expands what computing — and humanity — can achieve

We are committed to building a home for exceptional talent.

Optalysys

About the Role

Role: Staff Analogue IC Design Engineer – High-Speed Custom Logic
Department: IC Design / Hardware Engineering
Location: US (Hybrid / Onsite)
Employment Type: Permanent, Full-Time
Level: IC3.5 / IC4

The Staff Analogue IC Design Engineer will join a senior analogue design team responsible for pushing the performance limits of advanced CMOS technologies (≤45 nm). The role focuses on **hand-crafted, high-speed custom logic**, particularly **domino and dynamic logic architectures**, to implement arithmetic building blocks and ultra-deep pipelines operating near process limits.

The engineer will be responsible for **architecture, design, verification, and silicon correlation** of high-performance logic circuits and will collaborate closely with layout engineers to achieve optimal performance under real physical constraints.

Key Responsibilities

Architecture & Circuit Design

- Architect and design high-speed custom logic blocks including:
    - Serial and parallel adders
    - Modular arithmetic units
    - Shift registers
- Implement circuits using domino and dynamic logic techniques optimised for maximum speed.
- Perform device sizing and topology selection for critical logic paths.

Dynamic Logic Optimisation

- Design and optimise domino logic paths including:
    - Keeper strategies
    - Clock skew management
    - Charge sharing mitigation
    - Noise robustness
    - Setup and hold margin analysis

Performance & Timing Closure

- Achieve timing closure for ultra-deep pipelined logic structures.
- Conduct PVT corner analysis and statistical variation studies.
- Evaluate effects of process scaling, supply integrity, and interconnect parasitics.

Verification & Simulation

- Develop and maintain golden simulation testbenches.
- Perform mixed-signal and transient simulations using Spectre/APS.

- Conduct corner, Monte Carlo, and transient noise simulations.

Layout Collaboration

- Work closely with layout engineers to ensure parasitic-aware optimisation.
- Account for layout-dependent effects including:
  - Well proximity effects
  - Layout-dependent device variation (LDE)
  - Density and proximity impacts
  - Wiring parasitics

Methodology & Design Reviews

- Contribute to development of speed-optimized design methodologies.
- Participate in design reviews and sign-off processes.
- Define characterization methods and performance validation criteria.

Silicon Bring-Up

- Support silicon debug, validation, and correlation between simulation and measured silicon performance.

Required Experience & Skills

- MEng, MSc, or PhD in Electronic Engineering, Electrical Engineering, or a related field.
- 8–10+ years of experience in analogue or custom IC design.
- Proven domino/dynamic logic tape-outs in ≤45 nm CMOS nodes.
- Demonstrated design of high-speed arithmetic circuits such as adders, shifters, and modular arithmetic units.
- Strong understanding of device physics and performance trade-offs, including:
  - Threshold voltage and leakage
  - Body biasing
  - Device stacking
  - Interconnect RC effects
  - Supply integrity
- Extensive experience with Cadence Virtuoso design environment.
- Simulation using Spectre / APS.
- Experience with parasitic extraction tools (Quantus or StarRC).
- Scripting ability for automation and workflow improvements.
- Experience with silicon bring-up and debug.
- Ability to correlate simulation results with measured silicon data.

Preferred / Additional Experience

- Design of embedded memory blocks (SRAM or register files).
- Development of custom sense amplifiers.
- Experience with clock generation or timing circuits such as:
  - DLLs

- PLLs
- Experience with very high-frequency logic design methodologies.

Benefits

We offer competitive compensation. The base salary range for this role determined based on location, experience, educational background, and market data.

Salary Range: total compensation goes beyond base salary, it also includes comprehensive health care plan, retirement savings matching program, generous time off, annual performance-based bonus, and other rewards that recognise your impact and contribution.

$185,000 – $260,000

Benefits eligibility may vary depending on your employment status and location. Optalysys recruits, employs, trains, compensates, and promotes regardless of race, religion, color, national origin, sex, disability, age, veteran status, and other protected status as required by applicable law.

How to apply

Please send a copy of your CV to recruitment@optalysys.com with a cover letter