CMOS Layout Design Engineer – High-Speed Logic & Monolithic Photonics

Job Specification

About Optalysys

Optalysys is a pioneering UK and US based deep-tech company developing new ways to power the future of computing. By harnessing light, we are creating advanced photonic technologies that help the world's most demanding systems run faster and more efficiently. Our work supports breakthroughs in areas such as artificial intelligence, cybersecurity and scientific discovery. At Optalysys, we're bringing together talented people who are passionate about building technology that expands what computing — and humanity — can achieve

We are committed to building a home for exceptional talent.

Optalysys

About the Role

Role: CMOS Layout Design Engineer – High-Speed Logic & Monolithic Photonics
Department: IC Design / Physical Design
Location: Bangalore (Hybrid / Onsite)
Employment Type: Permanent, Full-Time
Level: IC3 / IC3.5

The CMOS Layout Design Engineer will be responsible for full-custom layout development from block-level through top-level integration for high-speed analogue and mixed-signal circuits as well as monolithically integrated photonics components in advanced CMOS nodes (<45 nm).

The role requires close collaboration with circuit designers to ensure parasitic-aware layout optimisation and to achieve aggressive performance, noise, and reliability targets. The engineer will also contribute to top-level floorplanning, ESD strategy implementation, and final tape-out sign-off.

Key Responsibilities

Custom Layout Development

- Implement full-custom layout for high-speed analogue and mixed-signal blocks including:
    - Arithmetic units
    - Data converters
    - References and bias circuits
    - High-current drivers
- Apply advanced layout techniques including:
    - Device matching
    - Common-centroid structures
    - Symmetry and gradient cancellation
    - Shielding and critical-net routing
- Optimise layouts for **low jitter, low noise, and minimal parasitic impact**.

Photonics Integration

- Support **monolithic photonics integration** within CMOS processes.
- Perform co-layout of electrical circuits and photonic elements including:
    - Heater drivers
    - Photonic monitoring diodes
    - Optical I/O placement
- Ensure compliance with photonics-specific constraints such as:
    - Optical keep-out regions
    - Thermal coupling considerations
    - Optical alignment requirements.

ESD & Padframe Design

- Implement **ESD protection strategies** according to foundry rule decks.
- Plan and integrate **I/O ring structures and padframes**.
- Ensure robust ESD protection while maintaining signal integrity for high-speed interfaces.

Top-Level Integration

- Perform **top-level floorplanning and hierarchical layout integration**.
- Manage physical design constraints including:
    - Guard rings
    - Well/substrate isolation
    - Noise coupling mitigation
- Coordinate block integration and routing at the chip level.

Tape-Out Execution

- Drive physical verification closure for tape-out, including:
    - DRC
    - LVS
    - Parasitic extraction (PEX)
    - Antenna checks
    - DFM compliance
    - Metal density and filler insertion
- Generate final sign-off packages for foundry submission.

Design Collaboration

- Work closely with circuit designers to enable **layout-aware circuit optimisation**.
- Support **engineering change orders (ECOs)** during late-stage design iterations.
- Provide feedback on layout-driven parasitic effects and performance trade-offs.

Required Experience & Skills

- HND, BEng, or MEng in Electronic Engineering, or equivalent industry experience.
- 5–8+ years of CMOS custom layout experience.
- Advanced-node experience, preferably 45 nm CMOS or smaller.
- Strong expertise in high-speed logic and analogue/mixed-signal layout techniques, including:
- Matching strategies
- Symmetry and common-centroid placement
- Shielding of sensitive nets
- Critical path routing.
- Proven experience implementing ESD protection schemes and I/O ring integration.

- Familiarity with foundry ESD rule decks and padframe reliability requirements.
- Proficiency in Cadence Virtuoso Layout XL / GXL.
- Experience with parasitic extraction tools such as Quantus or StarRC.
- Experience with physical verification tools such as Calibre or Synopsys ICV.
- Understanding of monolithic photonics integration constraints, including:
- Optical keep-out regions
- Thermal coupling
- Optical alignment considerations.

Preferred / Additional Experience

- Experience with layout automation using SKILL or Python.
- Familiarity with layout-driven circuit optimization techniques.
- Knowledge of reliability considerations, including:
    - Electromigration (EM)
    - IR drop
    - Latch-up prevention
- Experience designing padframes or high-current driver layouts.

Benefits

We offer competitive compensation. The base salary range for this role determined based on location, experience, educational background, and market data.

Salary Range: total compensation goes beyond base salary, it also includes comprehensive health care plan, retirement savings program, generous time off, annual performance-based bonus, and other rewards that recognise your impact and contribution.

Benefits eligibility may vary depending on your employment status and location. Optalysys recruits, employs, trains, compensates, and promotes regardless of race, religion, color, national origin, sex, disability, age, veteran status, and other protected status as required by applicable law.

How to apply

Please send a copy of your CV to recruitment@optalysys.com with a cover letter