



Senior High-Speed Custom Logic Design Engineer

Job Specification

About Optalysys

Optalysys is a pioneering global deep-tech company developing programmable silicon photonic Compute-in-Transit technology that enables operations to be performed directly within the data path, reducing movement overhead and creating new compute capability for data movement-bound infrastructure. Our work supports breakthroughs in areas such as artificial intelligence, cybersecurity, and scientific discovery.

At Optalysys we take on the hardest challenges to enable a future of limitless compute

A future where intelligence and light unlock what conventional computing cannot, accelerating discovery and expanding the possibilities of what computing can bring to all of us.

We're bringing together talented people who are passionate about building technology that expands what computing – and humanity – can achieve

We are committed to building a home for exceptional talent.



About the Role

Role: Senior High-Speed Custom Logic Design Engineer

Department: Engineering

Location: Leeds, UK (Onsite)

Employment Type: Permanent, Full-Time

Level: IC3

The Senior High Speed Custom Logic Design Engineer will own the architecture, transistor-level design and sign-off of timing-critical custom logic for a high-speed, compute-enabled PHY connecting photonic, analogue and digital subsystems.

The role will translate demanding requirements across throughput, latency, jitter, power and interface performance into robust custom circuit solutions, models and implementation collateral, taking designs from initial concept through layout, tapeout and first-silicon bring-up and debug.

Working closely with analogue, photonic and physical design engineers, the role will drive parasitic-aware circuit and layout optimisation to achieve aggressive targets for performance, noise, power, robustness and reliability.

This is a highly technical, hands-on role requiring deep expertise in high-speed custom logic design and the ability to make architecture and circuit-level trade-offs across complex mixed-signal systems.

Key Responsibilities

Custom Circuit Development

- Design high-speed logic circuits derived from behavioural models
- Define the microarchitecture and circuit specifications for high-speed custom logic, serializer and deserializer datapaths, clocking and control functions
- Design high-speed flip-flops, registers and memory banks
- Design transistor-level and schematic-based custom digital building blocks using appropriate static, dynamic and current-mode logic techniques
- Optimise performance across process, voltage, temperature, mismatch, extracted parasitics, signal integrity and reliability corners

Layout

- Guide custom layout, including critical-path placement, matching, shielding, clock distribution and power integrity, and close DRC, LVS and post-layout sign-off
 - Partner with layout engineers for parasitic extracted simulations
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Design Collaboration

- Work closely with the Director of Photonics to understand circuit requirements and architecture
- Create behavioural, timing and power models plus interface and characterisation collateral for RTL, verification, STA and physical design flows
- Support design reviews, tapeout sign-off, lab bring-up and first-silicon debug, working closely with analogue, photonics, verification and system teams
- Work closely with circuit designers and layout engineers to enable layout-aware circuit optimisation
- Support engineering change orders (ECOs) during late-stage design iterations
- Provide feedback on layout-driven parasitic effects and performance trade-offs

Personal skills and attitude

- Strong analytical and problem-solving skills, with the ability to think beyond conventional approaches.
- Embrace changes and challenges
- Adaptable to agile operations and start-up culture

Required Experience & Skills

- Degree in electronic engineering, microelectronics, computer engineering or a related discipline.
- Experience in custom digital or high-speed mixed-signal IC or DSP design experience, including multiple successful tapeouts.
- Strong understanding of transistor-level CMOS logic, high-speed datapaths, clocking, timing, power and signal-integrity trade-offs.
- Hands-on experience with Cadence Virtuoso and Spectre or comparable schematic, simulation and post-layout analysis tools
- Experience taking timing-critical custom logic from specification through layout sign-off, model delivery, tapeout and silicon debug

Preferred / Additional Experience

- Experience designing high-speed custom logic such as compressors, integrators, ALU, DSP or low-latency control paths
 - Experience with 7 nm, 12 nm or comparable advanced CMOS and FinFET technologies and mixed-signal interfaces
 - Knowledge of custom-cell characterisation, Liberty timing and power models, static timing analysis and RTL integration handoffs
 - Familiarity with flip-chip or multi-die integration, ESD, electromigration and power-integrity constraints
 - Knowledge of Verilog-A is advantageous
 - Python, Tcl or SKILL automation experience for design sweeps, model generation and sign-off reporting
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Benefits

We offer competitive compensation. The base salary range for this role is determined based on location, experience, educational background, and market data.

Salary Range: total compensation goes beyond base salary; it also includes comprehensive health care plan, employer contributed pension plan, generous time off, annual performance-based bonus, and other rewards that recognise your impact and contribution.

Benefits eligibility may vary depending on your employment status and location. Optalysys recruits, employs, trains, compensates, and promotes regardless of race, religion, color, national origin, sex, disability, age, veteran status, and other protected status as required by applicable law.

How to apply

Please send a copy of your CV to recruitment@optalysys.com with a cover letter
