



Senior RTL Design Engineer

Job Specification

About Optalysys

Optalysys is a pioneering global deep-tech company developing programmable silicon photonic Compute-in-Transit technology that enables operations to be performed directly within the data path, reducing movement overhead and creating new compute capability for data movement-bound infrastructure. Our work supports breakthroughs in areas such as artificial intelligence, cybersecurity and scientific discovery.

At Optalysys we take on the hardest challenges to enable a future of limitless compute

A future where intelligence and light unlock what conventional computing cannot, accelerating discovery and expanding the possibilities of what computing can bring to all of us.

We're bringing together talented people who are passionate about building technology that expands what computing – and humanity – can achieve

We are committed to building a home for exceptional talent.



About the Role

Role: Senior RTL Design Engineer

Department: Engineering

Location: Leeds, UK (Onsite)

Employment Type: Permanent, Full-Time

Level: IC3

The Senior RTL Design Engineer will lead RTL architecture and digital top-level integration for the control, data movement and protocol-facing logic surrounding Optalysys' photonic compute path.

You will define robust digital architectures and clean interfaces across serializers, side channels, custom memory, monitoring logic and external host protocols, translating system-level requirements into efficient, synthesizable RTL.

The role requires close collaboration with photonics, analogue, verification, physical design and layout engineers, taking designs from architecture through implementation, tapeout and first-silicon bring-up.

Key Responsibilities

Custom Circuit Development

- Design synthesizable RTL for control state machines, data paths, side channels and configuration functions
- Design synthesizable RTL for custom PCS and MAC sub-layers
- Define digital top architecture, clock and reset strategy, register maps and block level interfaces

Top level integration

- Integrate serializer interfaces, custom memory, analogue controls and host facing protocol adapters
- Develop lint, CDC, RDC, synthesis and formal checks and resolve issues before handoff to physical design

Design Collaboration

- Work closely with the Director of Photonics to understand circuit requirements and architecture
 - Create behavioural, timing and power models plus interface and characterisation collateral for RTL, verification, STA and physical design flows.
 - Support design reviews, tapeout sign-off, lab bring-up and first-silicon debug, working closely with analogue, photonics, verification and system teams
 - Work closely with circuit designers and layout engineers
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- Partner with verification engineers to build measurable requirements and close functional coverage
- Support FPGA prototyping, bring up, silicon debug and design updates after characterisation

Personal skills and attitude

- Strong analytical and problem-solving skills, with the ability to think beyond conventional approaches.
- Embrace changes and challenges
- Adaptable to agile operations and start-up culture

Required Experience & Skills

- Degree in electronic engineering, computer engineering or a related discipline
- Experience with high-speed serial data paths, CXL, PCIe, UCIe, AXI or AMBA interfaces
- Experience with memory interfaces, DDR5, LPDDR, or HBM
- At least 8 years of ASIC RTL design and digital top integration experience
- Advanced System Verilog or Verilog skills and strong understanding of synthesis and timing constraints
- Experience with clock domain crossing, reset design, low power methods and hardware debug
- Track record of working with mixed signal, custom logic and physical design teams through tapeout

Preferred / Additional Experience

- Knowledge of custom arithmetic, memory and low latency pipeline design
- Python, Tcl or build automation experience
- Experience in 7/12nm process
- Experience with Cadence EDA flow
- Any experience working with Photonics or high-speed interconnects

Benefits

We offer competitive compensation. The base salary range for this role is determined based on location, experience, educational background, and market data.

Salary Range: total compensation goes beyond base salary; it also includes comprehensive health care plan, employer contributed pension plan, generous time off, annual performance-based bonus, and other rewards that recognise your impact and contribution.



Benefits eligibility may vary depending on your employment status and location. Optalysys recruits, employs, trains, compensates, and promotes regardless of race, religion, color, national origin, sex, disability, age, veteran status, and other protected status as required by applicable law.

How to apply

Please send a copy of your CV to recruitment@optalysys.com with a cover letter
